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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,634	07/25/2003	An-Ru Andrew Cheng	TOP 298	9620

23995 7590 09/21/2005

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,634	CHENG ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/626,634, and Amendment filed on 07/14/2005. Claims 14-20 have been newly added. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being unpatentable by Balachandran et al. (US Patent 6,618,830).

2. As to claims 1 and 14 Balachandran discloses:

(1) An integrated circuit on a chip, comprising:

a substrate (col.1, ll.14-15); and

at least one scan chain disposed in the substrate (wafer), with scan cells connected to form a series chain (The scan cells are generally flip-flops or other similar logical elements existing between stages of combinational logic within the circuit modified to permit serial access, col.1, ll.18-21), each connection being formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer (col.1, ll.14-47; col.1, ll.52-61; col.6, ll.15-30; col.6, ll.50-63);

(14) An integrated circuit on a chip, comprising:

a substrate (col.1, ll.14-15); and

at least one scan chain disposed on the substrate, with scan cells connected by connecting lines to form a series chain (The scan cells are generally flip-flops or other similar logical elements existing between stages of combinational logic within the circuit modified to permit serial access, col.1, ll.18-21), each connecting line (scan cells allow an appropriately configured tester to apply and observe logical patterns at internal circuit nodes or nets, col.1, ll.23-25) being formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer (col.1, ll.14-47; col.1, ll.52-61; col.6, ll.15-30; col.6, ll.50-63).

3. As to claims 2-10 and 15-20 Balachandran describes:

(2), (15) The integrated circuit as claimed in claim wherein the assigned routing layer is a first metal layer (col.6, ll.50-63);

(3), (16) The integrated circuit as claimed in claim wherein the layout constraint limits the connection to passage through at least the first metal layer (col.4, ll.7-37; col.6, ll.15-30; col.6, ll.50-63);

(4), (17) The integrated circuit as claimed claim wherein the layout constraint limits the connection to passage through only the first metal layer (col.4, ll.7-37);

(5), (18) The integrated circuit as claimed in claim wherein the layout constraint limits each metal line of the first metal layer, to form the connection, to line width of critical dimension (CD) of the first metal layer (col.6, ll.15-30);

(6), (10), (19) The integrated circuit as claimed in claim wherein the layout constraint further limits any metal line of a second metal layer in the connection to a line width exceeding CD of the second metal layer (col.8, ll.24-55);

(7)-(9), (20) The integrated circuit, wherein the layout constraint further requires any plug (metal lead) of a plug layer linking two metal lines in the connection to be more than one (col.1, ll.52-61; col.6, ll.50-63).

Allowable Subject Matter

4. Claims 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

An integrated circuit on a chip, comprising at least one scan chain disposed in the substrate, wherein the integrated circuit further has an auxiliary routing net positioned in parallel beside the scan chain, the auxiliary routing net has metal lines of different lengths to replace one of the connections in the scan chain, and the auxiliary routing net does not function when the scan chain is originally formed.

Remarks

5. Mostly Applicant argues "Balachandran fails to teach or suggest ... that each connection is formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer." Examiner interprets that the

minimum dimension is a minimum distance or space between two metal leads within a particular circuit layer. The claim 1 is clearly define a minimum dimension provided by design rules.

Balachandran recites: using scan cells (by applying patterns of inserted via scan cells) (col.1, lines 32-36), a pruning module is operable to apply adjacency criteria algorithm (design rules in application) to the at least two nets (for example, two metal leads within a particular circuit layer may be shorted, col.1, lines 52-55) associated with each of the potential bridging faults. Adjacency criteria algorithm is generated in response to the design rules, where restrictions are by a physical database 70 that includes physical layout). (col.6, lines 16-31 and 45-63).

So, above passages in Balachandran correspond to "each connection being formed according to a layout constraint with a minimum dimension provided by design rules for assigned routing layer".

Examiner defined Applicant's arguments as none persuasive.

Accordingly **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VUTHE SIEK
PRIMARY EXAMINER